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Applicant(s): Kelley et al. Application No.: 10/809,535 Filed: 3/24/2004 Title: COMPOSITIONS AND METHODS FOR POLISHING COPPER Attorney Docket No.: 02009US	Art Unit: 1765 Examiner: Kin Chan Chen

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. § 1.132

That I, Mr. Lee M. Cook, declare the following:

1) That I am employed as the Director of Future Technology Opportunities for Rohm and Haas Electronic Materials CMP, Inc. ("Rohm and Haas" fka Rodel, Inc.); and that I have been employed at Rohm and Haas since 1992 in various roles. I am not named as an inventor in this application, although I have worked extensively in conjunction with the development of the abrasive-free or "reactive liquid" polishing solutions claimed in this application since I have been at Rohm and Haas.

2) Before joining Rohm and Haas, I had the following relevant positions: From 1979-1987, I was a research scientist at Schott Glass Technologies, Inc. From 1987-1992, I was a senior research scientist at Galileo Electro-Optics, Inc. In both positions, polishing is involved extensively in the glass products of the respective companies. I was intimately involved in the development and troubleshooting of polishing processes. In addition, I have conducted research into the polishing process and have published several papers in scholarly journals and made several presentations at scientific conferences concerning the subject. My research in the polishing field prior to joining Rohm and Haas was directed primarily to polishing of glass, but also involved metal polishing. Since joining Rohm and Haas, my research and development

work and efforts have been focused primarily on polishing of semiconductor materials. This research has resulted in the inventorship of more than fifty US patents in the polishing consumable field. I have been invited to present papers at domestic and international conferences in Japan and Korea relating to polishing and planarization of semiconductor materials.

3) My educational background is a B.A. degree in Chemistry from Grinnell College, in 1974.

4) That as a result of my education and experience, I consider myself, and am considered by my peers, inside and outside of Rohm and Haas, to be a person skilled in the technology relating to this application.

5) That I reviewed US Pat. No. 5,981,454 to Robert J. Small ("Small") that issued November 9, 1999; and specifically, the "CMP Metal Chemistry" section of column 6.

6) That Small at column 6, lines 4 to 6 states: "This type of polishing relies on the oxidation of the metal surface and the subsequent abrasion of the metal oxide surface with an emulsion slurry."

7) That the term emulsion in this sentence refers to a multi-phase system and that the conventional usage of "emulsion slurry" in polishing terminology is to imply a solid or abrasive phase is contained in the liquid.

8) That the two-part oxidation of the metal surface with subsequent "abrasion" of Small at column 6, lines 4 to 6 also implies an abrasive.

9) That Small at column 6, lines 14 to 16 states that under ideal conditions, rate of metal oxide formation equals rate of oxide polishing. This statement implies that the chemical solution oxidizes the metal surface and that an abrasive removes the oxidized metal surface.

10) That at column 6, lines 34 to 36, Small describes a detailed mechanism proposed by Kaufman, F.; J. Electrochem. Soc; 138(11), P 3460, 1991 ("Kaufman")—see atached.

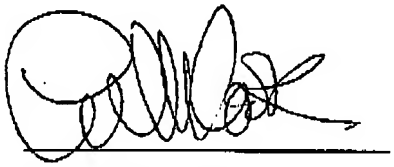
11) That in the paragraph bridging pages 3460 and 3461, Frank Kaufman uses the terms "absence of free abrasive" and "absence of added slurry" on an interchangeable basis.

12) That the paragraph of Kaufman bridging pages 3460 and 3461 describes the mechanism of absence of free abrasive as hydrodynamically assisted wet etching rather than

chemical-mechanical polishing. This places etching solutions outside the definition of polishing slurries.

13) That a skilled polishing slurry practitioner would understand that the term "emulsion slurry" as used in the context of Small refers to an abrasive-containing slurry.

14) That I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.



Mr. Lee M. Cook

September 26, 2007

Chemical-Mechanical Polishing for Fabricating Patterned W Metal Features as Chip Interconnects

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ABSTRACT

Interconnect features of W metal, recessed in an SiO_2 dielectric, can be formed using a novel chemical-mechanical polish process. Mechanical action, to continually disrupt a surface passivating film on W, and chemical action, to remove W, appear to be requirements for workability of the process. A trial process chemistry using a ferricyanide etchant is described. Removal of the W is discussed in terms of competition between an etching reaction which dissolves W and a passivation reaction to reform WO_3 on the surface of the W. This novel processing technology is compared with earlier methods of fabricating metal interconnect structures.

It is now generally recognized that planarization of multilevel metal interconnect structures for chips offers significant process advantages such as the elimination of step-coverage concerns and improvement of lithographic resolution by minimizing depth of field variations (1-7). Two alternative process approaches to achieving planarization can be considered (Fig. 1). One approach relies on dielectric planarization. In this case patterned metal interconnects are conformally covered with an insulator film. This is followed by a planarizing operation to eliminate the topography in the dielectric. Processes that have been used for smoothing include etch-back (8) of the dielectric, deposition of a planarizing polymer film (9), or chemical-mechanical polishing (10). Alternatively, recessed metal schemes (1-5) can be used where the reverse of the metal pattern desired is etched into a planarized film of dielectric, metal is conformally deposited, and then subsequently removed, in a separate step, from the higher blanket areas on top of the planarized dielectric to leave the required metal pattern recessed in the insulator.

An improved low-pressure chemical vapor deposition (LPCVD) process (11, 12) for tungsten, coupled with its high electromigration resistance and dry etch compatibility, makes it an attractive candidate for use in a recessed metal interconnection sequence (3, 5). However, current reactive ion etching (RIE) processes for tungsten which have been used to remove the blanket metal suffer from selectivity concerns due to resist thickness variations over the metal (3). Wet etching techniques are unacceptable due to their inability to preferentially remove topographic features.

Chemical-mechanical polishing (1, 2) could be used to define the tungsten features if a process chemistry appropriate for wafer fabrication were available. Chemical-mechanical polishing of metals has been demonstrated for stainless steels and nickel-based alloys (13), and for copper (2, 14). The mechanism we propose for the process (Fig. 2) requires the action of a metal etchant and a metal passivating agent with an abrasive agent. This combination could result in the high spots continually having the passivated film (anisotropically) etched away, while the low spots are protected. For the majority of metals, the oxide may be used as a simple passivant. During the process, the protective film is removed by the mechanical action of the abrasive slurry. This is followed by a rapid reformation of the protective film. Continuous cycles of formation, removal, and reformation of the passivating layer continue until the desired final thickness of metal is achieved.

Consideration of the proposed mechanism and Fig. 2 suggests that the minimal requirements for the proposed process chemistry for W removal are: (i) materials selectivity, a significantly faster removal rate for the W than either the dielectric surface, which forms the structure, or a sacrificial etch stop; (ii) topographic selectivity, a metal removal process which selectively removes metal from the "high" spots while leaving it protected in the low spots; (iii) the overall process should be noncorrosive, (iv) the process should leave the wafers clean enough to be compatible with further semiconductor processing in a clean room.

This paper will describe a process chemistry that has been successfully used in the chemical-mechanical polishing of tungsten to form chip interconnect structures using a recessed metal process sequence. Given the nature of the polish mechanism described, we suggest that the particular etchant-passivator combination discussed here is not the only chemical system that could be used for successful fabrication of interconnect structures. Preliminary descriptions of the application of this technology to form a fully planarized interconnect structure with 1.2 μm contacts, as applied to a 64 Kb complimentary metal oxide semiconductor static random access memory (CMOS SRAM), and, using x-ray lithography to achieve 0.5 μm on all interconnect levels, have previously appeared (6, 7).

Experimental

Materials and preparation of slurry.—All chemicals were used without further purification. Typical as-received purity levels were at least 98%. Water used in the preparation of the slurry had resistivities greater than 18 MΩ and was filtered through a Millipore filter system, type RO to remove ionic and organic contaminants and particles less than 1 μm in size.

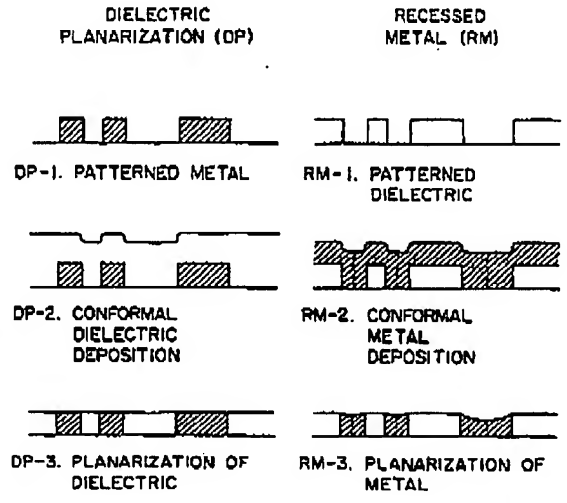

Fig. 1. Comparison of dielectric planarization (DP) and recessed metal (RM) approaches to the fabrication of chip interconnect structures.

* Electrochemical Society Active Member.

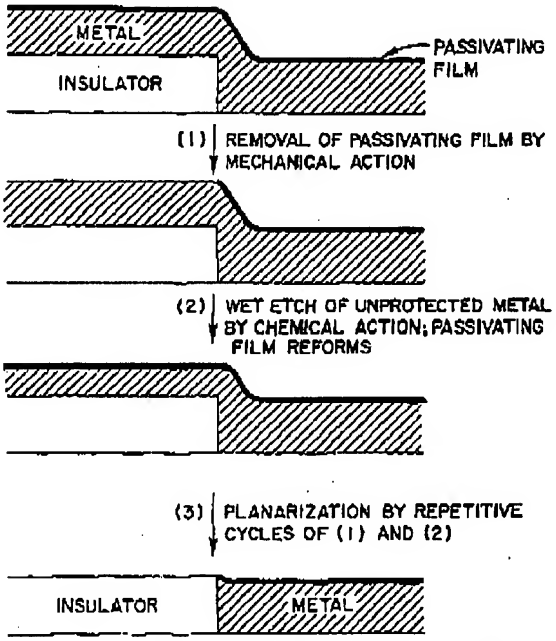

Fig. 2. Proposed mechanism of planarization of a patterned metal feature by chemical-mechanical polishing (see text for details).

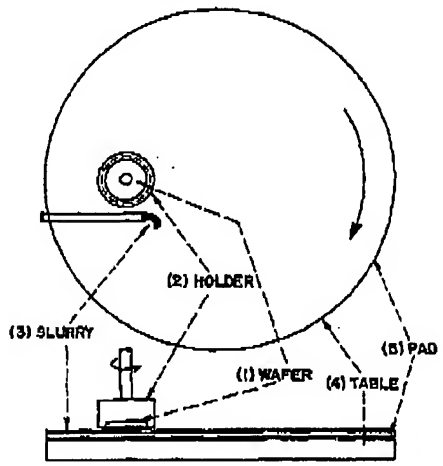

Fig. 3. Schematic of chemical mechanical-polishing technique, top and side views. For clarity, overarm mechanism connected to wafer holder has been omitted. Wafer (1) is held in holder (2) using commercially available template; slurry (3) flows between wafer surface and pad (5) covered table (4). See text for further details.

All slurries were prepared by adding the chemical constituents to a rapidly stirred solution of water. Addition of the abrasive to the solution typically resulted in the solution becoming optically opaque. To insure homogeneity of the polishing slurry, the resulting suspension was stirred during use. Although there was evidence for precipitate formation in the slurry after several hours, polish results were not found to change after storage for times up to 8 h. All slurries were delivered to the polish table using a peristaltic pump.

Slurry particle size analysis.—A Coulter Model LS 130 laser diffraction particle size analyzer was used to measure the particle size of the free abrasive in the polish slurry. Size calibration was checked using appropriate standards in the 0.1-100 μm particle size regime. Polish slurry particle sizes were determined on flowing samples (recirculation rates of 0.5 liter/min) using dilution factors (in water) in the 0.1 to 0.5 range.

Chemical-mechanical polish tools, fixtures, and operating parameters.—In general, we expect the same polish tools and fixturing traditionally used in the chemical-mechanical polishing of blanket Si wafers, to be applicable to the metal polishing process described in this work. In Fig. 3, is shown a schematic of the key components of the polish technique. The wafer (1) is placed in a holder (2) with the wafer surface in direct contact with a pad-covered table (4). During the polish experiment, the abrasive slurry (3) flows onto the surface of the pad and the rotation speed of the table and of the holder can be independently varied. Pressure at the wafer-slurry-pad interface is controlled via an overarm mechanism which allows pressures in the 1 to 5 kg/cm^2 range to be applied to the wafer holder. Most of the data presented here was obtained on Strasbaugh Model 6CA and 6DQ polishers but polish tools from other manufacturers are expected to be roughly equivalent in overall performance. Several different types of polish pad materials and wafer template assemblies obtained from Rodel were found to provide acceptable and reproducible results. Fixturing provided by other suppliers is expected to give similar results.

Si and W blanket and patterned substrates.—All polishing experiments were done on 125 mm Si wafers using an SiO_2 insulator layer. Following the deposition of a sputtered Ti/TiN adhesion layer, W was deposited using an LPCVD process (11, 12) in a batch CVD reactor (Genus 8402). Patterned wafers (6) for demonstration of the recessed W chemical-mechanical polishing process were prepared either by the Yorktown or East Fishkill Si Facility. These wafers had W deposited into RIE patterned features of a planarized SiO_2, with the planarization achieved using a previously described (10) chemical-mechanical polish process to smooth topographic variations in the SiO_2 insulator. Metallization consisted of RIE patterned Ti/Al(2.5%Cu)/Si deposited by dc magnetron sputtering. Argon sputter-cleaning was used prior to the metal deposition to insure adequate adhesion to the W and to the insulator surfaces.

W film thickness determination.—Average metal thickness and standard deviation was determined using either a manual four-point sheet resistivity probe apparatus or an automated four-point Prometrix Model 20 measurement tool. Thicknesses of the films were calculated from the experimentally measured sheet resistivity using the previously determined value for the layer resistivity (12) of the LPCVD W.

Determination of wet etch rates.—Removal rates of W were determined by comparing initial thicknesses (as determined above) of the W films *vs.* the thickness remaining after 1-24 h of contact with the liquid of interest. All results were determined for static solutions at 20°C.

Results and Discussion

In the absence of complexation reagents or substances which form insoluble salts, W becomes passivated at acidic pH values less than 4 (15) due to the formation of WO_3. However, in the presence of an oxidant such as $K_4Fe(CN)_6$ and weak organic base complexing agents, the range of pH in which W gets passivated is extended to 6.5 (16). Solutions were formulated containing the weak oxidant $K_3Fe(CN)_6$, and it was observed that by adjusting the pH, both low static wet etch rates and chemical-mechanical polish removal of W films could be simultaneously achieved, see Table I.

We observed that when the chemical formulations were combined with silica or alumina abrasive particles, W films could be chemical-mechanically polished at removal rates as high as 400 nm/min. For the formulations listed in Table I with pH values less than 6.5, the W removal rates obtained were found to be functions of the "mechanical" components of the process, *viz.*, rates increased with applied pressure, quill/table rotation speeds, and increased

Table I.

Formulation (Note 1)	pH	Wet etch rate (nm/sec)	CMP observed (Note 2)
K-F	5.0	8	+
K-F-En	6.5	6	+
F-En	10.5	43	–

F = $K_3Fe(CN)_6$; K = KH_2PO_4; En = Ethylenediamine.
1. Formulations typically contain 0.1-5 weight percent of chemicals.
2. Chemical-mechanical polishing (CMP) and pH determined on formulations containing abrasive. (See text for details.)

loading of abrasive. In the absence of applied pressure or free abrasive, the W removal rates were found to be minimal. This implies that areas of recessed metal would only be slowly removed. However, for the chemical formulation with pH 10.5, significant removal rates were found in the absence of added slurry or applied pressure suggesting, in this case, a removal process which is hydrodynamically assisted wet etching rather than chemical-mechanical polishing.

The optimum particle size and particle size distribution for the abrasive additive has not been determined. However, we have observed that commercially available colloidal silica or dispersed alumina in the 0.2-2.0 μm size range (see Experimental section) yield W surfaces after polishing that are highly specular and which appear scratch-free to the human eye. In Fig. 4 is shown particle size data for an alumina dispersion. We find that for any of the process chemistries in Table I, the measured particle size and distribution stays relatively constant. Although the alumina is specified as a deagglomerated solid with 0.05 μm average particle size, the light scattering measurements suggest that in the flowing, liquid state, the average particle size is considerably larger. Whether alumina aggregates form in solution and subsequently break apart during the polishing operation is not known at present. We have observed that addition of a coagulation agent to the slurry results in immediate settling of the normally dispersed fine particulates. Particle size analysis performed on these coagulated samples show significantly larger measured particle size, in addition to a distinct increase in surface scratching of the metal films polished under these conditions. This suggests a potentially important relationship between average particle size at the wafer surface and the incidence of polish-induced damage at that surface.

Further distinction between removal of a blanket W film under chemical-mechanical polish conditions *vs.* wet etching (when process chemistry pH is above the passivation limit) can be made by observing the thickness decrease over the surface of the wafer as a function of polish process time. In Fig. 5 are shown two traces where W thickness is plotted over multiple points on the wafer surface before (a) and after (b) 3 min of polish processing in the chemical-mechanical polish mode. Two effects are observed which reflect the novel aspects of the removal process. It is seen that during the polishing, in addition to a thinning of the metal film as a function of time, the thickness uniformity of the metal can be modified. In the specific example shown in the figure, after 3 min of polishing at 130 nm/min the original film, which was lower in the center, now has a

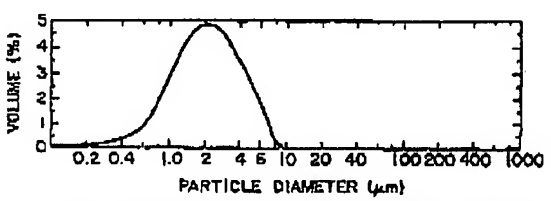

Fig. 4. Particle diameter in microns vs. volume percent population for an alumina slurry in the F-K-En chemistry as determined by light scattering.

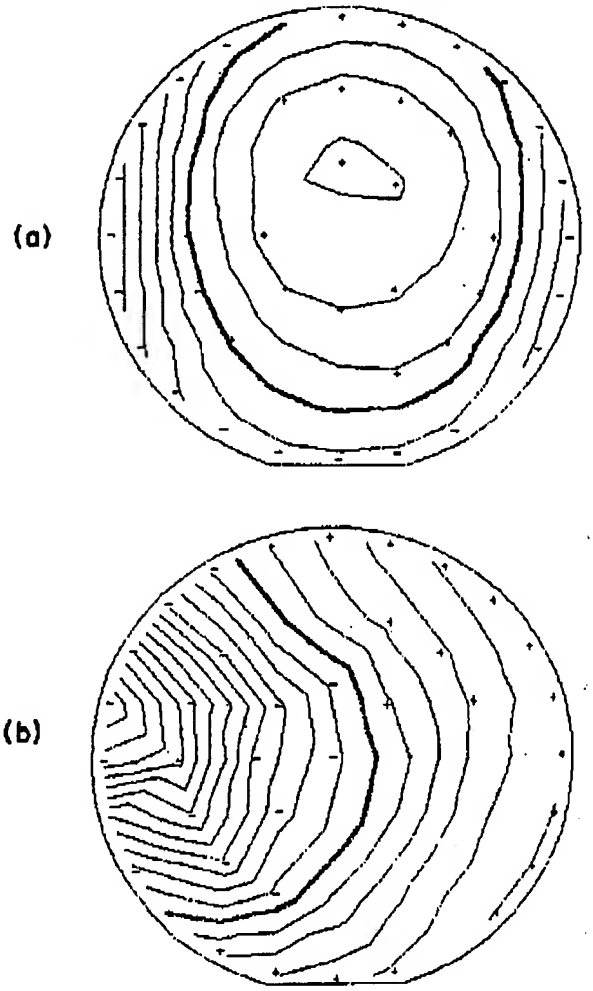

Fig. 5. Sheet resistivity contour maps of blanket W films, where lines connect measured points of constant resistivity. Bold solid lines give mean resistivity with dotted lines showing areas which have higher (+) or lower (−) sheet resistivity than the mean. (a) Initial film with mean, calculated, thickness of 500 nm; each contour interval (dotted line) has successively 4% higher or lower sheet resistivity than the mean. (b) after 3 min polishing, mean thickness 112 nm with 8% deviation per contour line.

wedge shape with the maximum to minimum thickness variation observed from one wafer edge to another. In general, we have found that many different kinds of final global planarity can be achieved, dependent on the initial thickness uniformity of the metal film and the settings of the polish tool. Experiments done using identical polish tool settings but with the F-En chemistry at pH 10, show an isotropic removal of W, with no change in the global planarity of the film, typical of a wet etching process.

In addition to the sensitivity of the removal process to choice of mechanical parameters during polishing, as mentioned above, we find that the polish rates also depend on the concentration of chemicals listed in Table I and on the temperature of the slurry during processing. This suggests, consistent with the proposed mechanism, that the polish process is driven both by mechanical and by chemical effects. We typically observe that polish rates are proportional to the concentration of chemical constituents listed in Table I. In addition, we find that at any given concentration of chemicals, polish rates increase as a function of increasing temperature of the slurry. By controlling the temperature of the recirculating water which flows through the polish table the temperature of the slurry con-

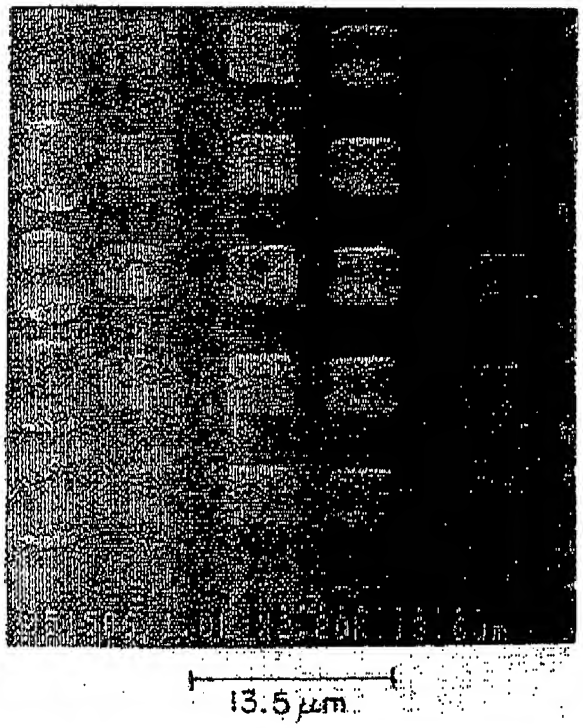

Fig. 6. SEM views of a patterned W in SiO_2 dielectric surface following chemical-mechanical polishing.

tacting the wafer surface can be controlled. Given the hydrodynamic and chemical complexity of the polishing process, we suggest that modeling of the concentration and thermal effects observed will have to take into account a number of competing processes. These include diffusion to and depletion of the chemical constituents at the wafer interface, the kinetics of passivating film formation, and the dynamic rate of isotropic wet etching (see below) prior to the formation of the passivating film.

This process can readily be applied to form W vias in an SiO_2 insulator layer (6, 7). A typical process sequence involves deposition of the insulator layer followed by lithographic patterning of the insulator, sequential deposition of both an adhesion layer and blanket W, followed by polishing to remove the surface W. Figure 6 is a scanning electron micrograph top down view of W patterns that result after processing. We observe that the patterned metal is well defined with no evidence of metal smearing into the adjacent insulator. In addition, the surface of the W is highly specular without any obvious chemical attack or corrosion.

Cross-sectional scanning electron micrograph (see Fig. 7) shows clear evidence for the planarity of the process and indicates that the W seams, unavoidable with a conformal CVD deposition process, have not been degraded by process induced wet etching. In general, we find that the degree of local planarity (metal *vs.* insulator height) and the final thickness and uniformity of the insulator film is dependent on the removal rate ratio of metal-to-SiO_2 insulator.

However, we have observed that subtle changes made to the process chemistry can lead to a degradation in quality of the recessed metal surface. This is an effect only observed on patterned wafers since blanket, polished films are always smooth. On blanket W wafers the K-F chemical system, with or without the addition of ethylenediamine, shows very similar blanket polish rates, and low static wet etch rates suggesting efficient surface passivation. Patterned wafers polished with the K-F-En chemistry show high-quality cross-sectional SEM features similar to those in Fig. 7. However, patterned wafers polished under exactly the same conditions and using the K-F chemistry in the absence of ethylenediamine show distinct signs of surface attack and loss of planarity relative to the adjacent insulator surface. This observation suggests that in the presence of ethylenediamine, and under the dynamic conditions of polishing, surface passivation of W is more efficient than in the absence of the weak amine base. The mechanism proposed for W passivation in the presence of ferricyanide involves (16), see Eq. [1]

$$W + 6Fe(CN_6^{-3} + 4H_2O \rightarrow WO_4^{-2} + 6Fe(CN)_6^{-4} + 8H^+ \quad [1]$$

the generation of protons at the surface via a W/W^{+6} redox reaction. The local concentration of protons at the metal interface can be expected to be influenced by the presence of buffering agents and weak base. We, therefore, suggest that static wet etch rates and bulk solution pH values alone do not entirely reflect the dynamic chemical environment which occurs at the metal-solution interface during metal polishing.

Fully planarized, two level interconnect structures, with W studs forming the contacts to the underlying Si device areas and between the wiring levels *i.e.* (W stud1-M1-W stud2-M2), have been recently fabricated (6, 7). The W stud levels were formed in a chemical-mechanical polish process using the K-F-En process chemistry. Overall yields were high and contact resistance values were not affected by the chemical-mechanical polish processing. The data show, see Fig. 8, the contact resistance scales with feature

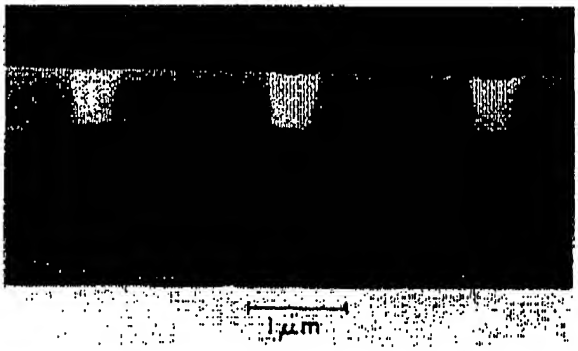

Fig. 7. Cross-sectional SEM view of W studs in SiO_2 insulator.

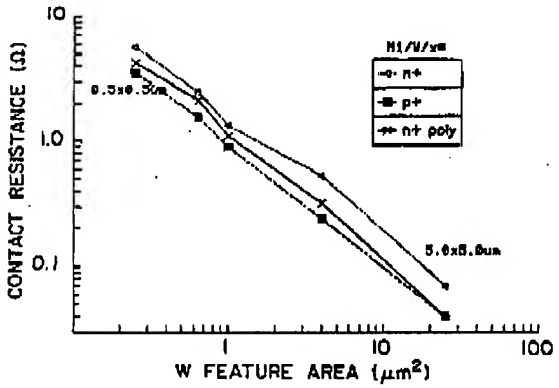

Fig. 8. Contact resistance of W contacts recessed in an SiO_2 dielectric for feature sizes from 0.5 to 5.0 μm². Comparison made for W contacts from Ti/Al(2.5%Cu)/Si M1 to silicided n⁺, p⁺, and to n⁺ polysilicon chip regions.

area for 0.5 to 5.0 μm² contacts. This indicates either the absence of significant polish-induced contamination at the interface or that the surface contamination produced does not survive the sputter-clean step performed prior to metall deposition (see the Experimental section). M1-M2 via resistances were appropriately lower due to the absence of the silicide. An improved W chemical-mechanical polishing process was used to fabricate a 4 Mbit DRAM (17) structure using a CVD-tungsten bit line and contacts in a dual damascene (18) process in manufacturing.

A consequence of the low contact resistance values observed for the W interfaces and the proposed mechanism of chemical-mechanical polishing is the presence of a chemically passivating layer on the surface of the polished tungsten. XPS and Auger analysis of polished CVD blanket W samples confirms (19) the presence of a thin layer of tungsten oxide. It is estimated that the oxide consists of 5-6 Å of WO_2 over 3-10 Å of some other lower oxidize that forms a transitional region between the WO_2 and the bulk W. Furthermore, there was no evidence to indicate the presence of any significant post polish residue or other impurities.

We propose that the chemical-mechanical polishing of W proceeds initially (see Fig. 2) by the abrasive removal of this protective thin oxide film. Once the unpassivated surface of the W film is exposed by the mechanical process, the W is removed by the chemical activity of the ferricyanide/hydrogen-phosphate/ethylenediamine combination. In this interpretation, ferricyanide acts as an electron sink to oxide and solubilize the W as a WO_4^{-2} specie (see reaction [1]). Competing with this etching reaction is reaction [2], to reform a new layer of the passivating oxide

$$W + 6Fe(CN)_6^{-3} + 3H_2O \rightarrow WO_2 + 6Fe(CN)_6^{-4} + 8H^+ \quad [2]$$

Direct evidence for the intermediacy of the Fe(III) moiety and its consumption during polishing is obtained by observing the color changes which occur during the polish process. For example, when polishing a blanket W wafer we observe that the initial yellow color of the ferricyanide species is replaced, while the W is being consumed, by a much more colorless, opaque, solution. Following complete removal of the W, the yellow color seen initially reappears. We interpret these color changes to mean that while W is being actively dissolved (reaction [1]) or consumed to form a new passivating layer (reaction [2]), the colored Fe(III) species rapidly reacts to form the colorless Fe(II) reduction product. Once all the W is removed in the polish process, the concentration of the Fe(III) species again increases and the original color returns. In this interpretation, the ferricyanide is responsible for the oxidation of the W, while the hydrogen phosphate buffer-ethylenediamine base combination acts, at the W-solution interface, to control the local pH. Thus once the passivating film is disrupted by a mechanical event, at a given dynamic concentration of ferricyanide oxidant, the competition between the etching and passivation reactions is determined by the interfacial concentration of buffer and weak base. High quality, patterned surfaces of W can only be achieved when there is the appropriate dynamic balance between the W etch and passivation effects.

Conclusions

A chemical-mechanical polish process for the removal and planarization of W films is described. The process involves polishing with a mixture of ferricyanide-phosphate in the presence of free abrasive particles. Mechanical action to continually remove a passivating film, and chemical action to dissolve W and reform the passivating film appear to be requirements for process feasibility. Global planarity using the polish process is achieved, a result not obtainable using isotropic wet chemical etch processes. Static wet etch rates determined on blanket films and process chemistry pH appear to be useful ways of predicting chemical-mechanical polishing activity. However, polishing of patterned wafers has shown chemistry-dependent surface defects in recessed areas, a problem overcome with the addition of ethylenediamine, which could not be detected on blanket wafers alone.

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Effects of Microstructure and As Doping Concentration on the Electrical Properties of LPCVD Polysilicon

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ABSTRACT

The microstructure and electrical properties of polysilicon films deposited by low-pressure chemical vapor deposition on silicon dioxide have been investigated as a function of deposition condition and As doping concentration. The deposition temperature was varied from 560°C to 625°C, and the As doping concentration from 1×10^{17} to 5×10^{20}/cm³. The polysilicon films deposited at 625°C and annealed at 900°C have an average grain size of 200-300 Å and a rough surface with columnar grain structure, while the films deposited at 560°C followed by the 900°C anneal have 1000 Å grains and smooth surfaces. For the same As doping concentration, the conductivity and Hall mobility of the polysilicon deposited at 560°C are larger than those of the polysilicon deposited at 625°C, due mainly to less grain boundary trapping. The grain boundary potential barrier decreases from 0.063 eV in films with As doping concentration of 5×10^{18}/cm³ to 0.001 eV in films doped to 2.5×10^{20}/cm³. The trap density of the grain boundary, however, is almost independent of the deposition conditions and the values are determined to be $3.6\text{-}5 \times 10^{12}$/cm².

Polycrystalline silicon (polysilicon) is widely used in very large scale integrated semiconductor technology. Heavily doped polysilicon is used as gate electrode and interconnection, while lightly doped polysilicon is used for resistors in static memory devices. Polysilicon with large grains is suited for the fabrication of low-cost solar cells. The electrical resistivity of polysilicon is, in general, larger than that of single-crystal silicon due to the existence of grain boundaries. It is reported (1, 2) that the dopant segregation at grain boundaries can affect the resistivity of polysilicon (dopant-segregation model). On the other hand, the Hall mobility minimum often observed in polysilicon with an intermediate doping level can hardly be explained by the segregation model only. The presence of a minimum in the mobility *vs.* doping concentration diagram was explained in terms of carrier trapping at grain boundaries (grain boundary trapping model) (3, 4). It has been reported that the microstructure of polysilicon films depends on the deposition and annealing temperatures (5), dopant concentration (6), and film thickness (7).

Recently, the surface smoothness of polysilicon films became another important factor, because polysilicon with a smooth surface can better serve as a substrate for the deposition of ultrathin layers of silicon dioxide or nitride in the fabrication of capacitors in ultralarge scale integrated devices and polycrystalline thin film transistors. Therefore, there is an interest in investigating the effects of deposition conditions and dopant concentration on the microstructure and electrical properties of low-pressure chemical vapor-deposited (LPCVD) polysilicon and in developing polysilicon films with smooth surfaces and various conductivities. In this paper, we report the results of an investigation of effects of deposition temperature and As dopant level on microstructure, carrier concentration, and Hall mobility in polysilicon films deposited on silicon dioxide grown on (100) silicon wafer.

Experimental

The equipment used to prepare polysilicon films in the present investigation was the same as that used for the production of mega-bit dynamic random access memory. Silicon dioxide layers of 1000 Å were formed by thermal oxidation at 900°C using a H_2/O_2 atmosphere on p-type, 6-9 Ω · cm, (100) wafers. Polysilicon films with a thickness of 0.25 μm were deposited on the oxide layers by LPCVD with a SiH_4 flow rate of 150 sccm. Two sets of films were prepared at two different deposition temperatures, 560°C and 625°C. Both sets of films were doped with As implanted in a dose range from 2.5×10^{12} to 1×10^{16}/cm². Then, an oxide layer of 3000 Å was deposited on the As-doped polysilicon films by CVD at 430°C to prevent the out-diffusion of the As dopant during subsequent annealing. The top oxide films were etched using a photomask to define the contact for van der Pauw patterns. For good

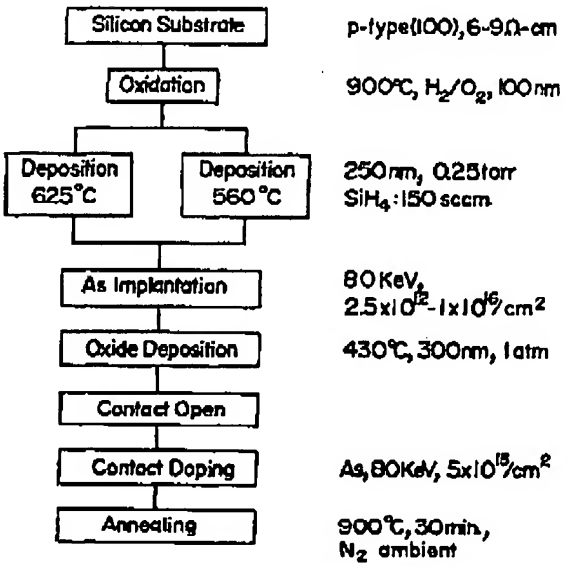

Fig. 1. Process flow chart for sample preparation.